AMENDMENT TRANSMITTAL LETTER (Large Entity)

Applicant(s): **Kerim Kalafala, et al.**

Docket No.: **FIS9-2003-0267-US1**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/665,273	09/18/2003	Binh C. Tat	32,074	2825	5468

Invention: **SYSTEM AND METHOD FOR CORRELATED PROCESS PESSIMISM REMOVAL FOR STATIC TIMING ANALYSIS**

COMMISSIONER FOR PATENTS:

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST # PREV. PAID FOR		NUMBER EXTRA CLAIMS PRESENT		RATE	ADDITIONAL FEE
TOTAL CLAIMS	30	-	30	=	0	x	$50.00	$0.00
INDEP. CLAIMS	3	-	3	=	0	x	$200.00	$0.00
Multiple Dependent Claims (check if applicable) ☐								$0.00
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT								$0.00

☒ No additional fee is required for amendment.

☐ Please charge Deposit Account No. _____ in the amount of _____

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- ☒ Any additional filing fees required under 37 C.F.R. 1.16.
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/H. Daniel Schnurmann/
Signature

Dated: **May 11, 2006**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE	
In re application of: **Kerim Kalafala, et al.**	Date: **May 11, 2006**
Serial Number: **10/665,273**	Examiner: **Binh C Tat**
Filed: **9/18/2003**	Group Art Unit: **2825**
Title: **System and Method for Correlated Process Pessimism Removal for Static Timing Analysis**	IBM Corporation D/18G, B/321, Zip 482 2070 Route 52 Hopewell Junction, NY 12533-6531

AMENDMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Responsive to the Office Action dated March 9, 2006, the following Amendment is being submitted to place the above-identified application in prima facie condition for allowance.

Kindly amend the above identified application and consider the following remarks:

IN THE CLAIMS:

Please amend the following claims:

1. (currently amended) A method for performing a static timing analysis of a digital system in the presence of a plurality of global sources of delay variation comprising the steps of:

a) selecting, for at least one timing test, at least one pair of an early path and a late path leading to said timing test;

b) identifying at least one global parameter ~~which the delays~~ on which distinct portions of said early and late paths' delays depend on;

c) determining for at least one of said global parameters at least one consistent value assignment; and

d) computing for each said consistent assignment a slack value for said path pair.

2. (original) The method as recited in claim 1 wherein one of said early and late paths is a clock path and the other of said early and late paths is a data path.

3. (original) The method as recited in claim 1, wherein said at least one timing test comprises those timing tests within said digital system whose slack falls below a specified threshold after an initial static timing analysis

4. (original) The method as recited in claim 1, wherein said identified path pair comprises a late critical path to said timing test and an early critical path to said timing test.

5. (original) The method as recited in claim 1, wherein said initial static timing analysis is performed using bounding parameter values.

6. (original) The method as recited in claim 1, further comprising the step of determining for each of said timing tests the worst of said computed slacks.

7. (original) The method as recited in claim 1, wherein said step c) further comprises the steps of:

e) enumerating combinations of realizable values of at least one of said identified parameters; and

f) performing a timing analysis for each of said enumerated combinations.

8. (original) The method as recited in claim 7, wherein said step e) is terminated after one of the timing analyses of step f) produces a slack below a specified threshold.

9. (original) The method as recited in claim 7, wherein at least one parameter whose realizable values are enumerated comprises a subset of the parameters identified in step b).

10. (original) The method as recited in claim 9, wherein said step e) is repeatedly applied to additional ones of said identified parameters until said step f) results in a slack which is greater than a specified slack threshold.

11. (original) The method as recited in claim 1, wherein said step b) further comprises identifying parameters in which delay functions are separable, and said step c) further comprises setting independently each of said parameters in which delay functions are separable to the value that results in the worst slack value at said timing test.

12. (original) The method as recited in claim 11, wherein said step of independently setting parameter values further comprises the steps of:

e) summing along the early and late paths of said path pair sensitivities of delay elements with respect to each of said parameters in which delay functions are separable;

f) computing the difference between said summed path sensitivities of said early and late paths, and

g) determining a value of each of said parameters in which delay functions are separable according to an arithmetic sign of said difference of sensitivities.

13. (original) The method as recited in claim 6, further comprising the step of determining whether the slack of any other early and late path pair to said timing test is worse than said determined worst slack, and if so, repeating said steps b), c), and d) for said other path pair.

14. (original) The method as recited in claim 1, wherein the timing analysis is performed at a gate-level.

15. (original) The method as recited in claim 1, wherein the timing analysis is performed at a transistor-level.

16. (original) The method as recited in claim 1, wherein the delay models are stored as pre-determined tables.

17. (original) The method as recited in claim 1, wherein the delay models are stored as pre-determined analytic equations.

18. (original) The method as recited in claim 1, wherein the delay models are computed on the fly.

19. (original) The method as recited in claim 1, wherein the circuit comprises a plurality of clock domains.

20. (original) The method as recited in claim 1, wherein the circuit is selected from the group consisting of at least one of the following clock configurations: mesh network, tree network, hybrid network, gated clocks and pulsed clocks.

21. (original) The method as recited in claim 1, wherein the sources of variability include a mistrack between one or more of the following device families that is selected from the group consisting of devices having different threshold voltages, devices having different gate oxide thicknesses and devices having different characteristics for PFET and NFET devices.

22. (original) The method as recited in claim 1, wherein the sequential elements are selected from the group consisting of at least one of: master-slave latches, flip-flops, edge-triggered latches, level-sensitive latches and transparent latches.

23. (original) The method as recited in claim 1, wherein the timing analysis is conducted for timing verification at one or more levels selected from the group consisting of a circuit level, macro level, functional-unit level, chip level, board level and system level.

24. (original) The method as recited in claim 1, wherein the circuit being analyzed is selected from the group consisting of at least one of the following technologies: CMOS, domino, static logic and dynamic logic.

25. (original) The method as recited in claim 1, wherein the global sources of variation include one or more of manufacturing variations, device fatigue variations, environmental variations, modeling variations, and circuit operation variations.

26. (original) A system for performing static timing analysis of a digital system in the presence of a plurality of global sources of delay variation comprising:

a) means for selecting, for at least one timing test, at least one pair of an early path and a late path leading to said timing test;

b) means for identifying at least one global parameter ~~which the delays~~ on which distinct portions of said early and late paths' delays depend on;

c) means for determining for at least one of said global parameters at least one consistent value assignment; and

d) means for computing for each said consistent assignment a slack value for said path pair.

27. (original) The system as recited in claim 26, wherein element c) further comprises:

e) means for enumerating combinations of realizable values of at least one of said identified parameters; and

f) means for performing a timing analysis for each of said enumerated combinations.

28. (original) The system as recited in claim 26, wherein said element b) further comprises means for identifying parameters in which delay functions are separable, and said element c) further comprises means for setting independently each of said parameters in which delay functions are separable to the value that results in the worst slack value at said timing test.

29. (original) The system as recited as recited in claim 28, wherein said means of independently setting parameter values further comprises:

e) means for summing along the early and late paths of said path pair sensitivities of delay elements with respect to each of said parameters in which delay functions are separable;

f) means for computing the difference between said summed path sensitivities of said early and late paths, and

g) means for determining a value of each of said parameters in which delay functions are separable according to an arithmetic sign of said difference of sensitivities.

30. (currently amended) A program storage device readable by a machine, tangibly, embodying a program of instructions executable by the machine to perform method steps for performing static timing analysis of a digital system in the presence of a plurality of global sources of delay variation, said method steps comprising:

a) selecting, for at least one timing test, at least one pair of an early path and a late path leading to said timing test;

b) identifying at least one global parameter ~~which the delays~~ on which distinct portions of said early and late paths' delays depend on;

c) determining for at least one of said global parameters at least one consistent value assignment; and

d) computing for each said consistent assignment a slack value for said path pair.

REMARKS

Claims 1-30 remain pending in the application. Claims 1, 26 and 30 have been amended.

Claims 1-30 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Hathaway et al. (U.S.P. 5,636,372) (Hathaway).

Applicants submit that theirs teaching is novel and is not taught nor suggested by Hathaway et al. Accordingly, Applicants traverse the above rejection for the following reasons:

The Office Action states in item 3, page 2

"As to claims 1, 26, and 30, Hathaway et. al. teach a method for performing static timing analysis of a digital system in the presence of a plurality of global sources of delay information, comprising the steps of a) selecting for at least one timing path one pair of early path and late path leading to said test. b) identifying at least one global parameter which the delays of said early and late paths depend on (fig 3, fig 4, fig 5, col 5 line 43 to col 7 line 46)

Applicants contend that Hathaway et al. teach a method where "the difference between early and late arrival times at the common path point (CCPPS) element which tags A," (col 6, lines 60-61) is the pessimism that is eligible to be removed for a specific path-pair. The CCPPS element (a timing point), however, is not a global parameter on which delays depend. Thus, Applicants believe that their teaching is distinct and novel when compared to that taught by Hathaway et al.

Notwithstanding, Applicants submit that in order to advance the prosecution of the present application, they opt to introduce the following limitation in claim 1 in order to further distinguish their invention from that of Hathaway et al., by clearly reciting in step b) "*identifying at least one global parameter on which distinct portions of said early and late paths' delays depend on;*."

Still in item 3), regarding the statement addressing step d0 of claims 1, 26 and 30:

d) computing for each said consistent assignment a slack value for said path pair (fig 4, fig 5, col 8 line 40 to col 10 line 18)

Applicants submit that Hathaway et al. describe separate propagations of arrival times from different CCPPS points, and comparison of consistent pairs of such propagated arrival times to compute slacks. However the sense in which consistency is determined is clearly different between Hathaway et al. and the present invention. Hathaway et al. teach that the consistency is dictated by whether or not the propagated arrival times are tagged with (i.e., were propagated from) the same CCPPS point. In the present invention consistency is clearly stated in step c) of claims 1, 26 and 30 to teach consistent values of a global parameter. And as noted above, a global parameter in the present invention is different from a common path point (CCPPS) as taught by Hathaway et al.

Since all the remaining rejections listed under items 4-27 of the Office Action relate to claims that are dependent of claim 1, 26 and 30, Applicants submit that Hathaway et al. do not teach "identifying at least one global parameter on which distinct portions of the early and late path delays' depend on", and thus are not anticipated by Hathaway et al.

To prove further the point above mentioned, Applicants have opted to select from among all the dependent claims the rejection found in item 9*), page 3 of the Office Action referring to claim 7 and 27, namely:*

"Hathaway et. al. teach wherein said step c) further comprises the steps of: e) enumerating combinations of realizable values of at least one of said identified parameters, and f) performing a timing analysis of said combinations."

Applicants contend that Hathaway, et al. teach a method where in "the difference between early and late arrival times at CCPPS element which tags A," (col 6, lines 60-61) is the pessimism that is eligible to be removed for a specific path-pair. The CCPPS element (a timing point), however, is not a global parameter on which delays depend.

Thus, Applicants submit that the amended claims 1, 26 and 30 and all claims dependent thereof are patentably distinct from Hathaway et al., and respectfully request that the Examiner reconsider and withdraw the rejection of the stated claims based on 35 U.S.C. 102(b)

Accordingly, Applicants believe that all the active claims are now in condition for allowance, and respectfully request that the Examiner enter the amended claims; that all the rejections and objections to this application be reconsidered and withdrawn; and that the Examiner pass all the pending claims to issue.

Should the Examiner have any suggestions pertinent to the present application, the Examiner is encouraged to contact Applicants' undersigned representative at the number shown below.

Respectfully submitted,
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